Abstract—In current trend for portable wireless communication applications, we require high Q on-chip inductors. In this paper an on-chip 3-D spiral inductor is proposed. High quality factor is achieved by reducing oxide capacitance between substrate and conductor considering permittivity of a substrate. Losses in the structure are reduced by considering high conductivity material like copper or gold. In this paper, 3-D inductor model is designed based on multi turn inductor concept embedded using multilayer CMOS topology. The proposed inductor is rectangular in geometry having maximum quality factor nearly 270 with inductance of 132nH at 40MHz frequency. Realization of designed inductor is done by using IE3D EM filed solver with the help of basic lumped pi-model. Proposed inductor is compared with the basic on-chip planar inductor model. In comparison proposed inductor shows better results than basic model in terms of Quality factor and Inductance. The proposed on-chip 3-D inductor has (47-162) % in terms of Q-factor and an improvement of (18-28) % inductance value in the frequency range of (30-100) MHz w.r.t planar inductor. The proposed high Q- inductor can be used in various wireless applications for RF and microwave subsystems. On-chip area of proposed inductor is 10x10mm².

Key words: Inductance, IE3D, Onchip inductor, Quality factor, wireless.

I. INTRODUCTION

In conventional wireless communication we use passive components which are surface surface-mounted devices occupy large on-chip area and leads to increase in cost. Optimization of inductor in terms of area can be done by integrating active or passive components on same silicon chip [1] [2] [3]. By using layout optimization techniques high Q on-chip inductors are proposed for wireless applications [4]. Wireless applications require low power, low noise and narrow bandwidth [5].

High Q-inductors of value 25-30 are proposed using conducting materials like copper and also with the help of multi level interconnects [6] [7]. Metal losses incurred while designing an inductor are supplemented using materials like copper or gold instead of aluminum [8]-[9]. Losses in on chip inductors are generally classified in to two types. They are losses due to capacitive coupling between metal windings to substrate and eddy current effects in the substrate layer. Several methods are introduced to reduce the losses for on-chip inductor to increase the value of quality factor.

The proposed 3-D inductor uses thick oxide layers to decouple the inductor and low resistive materials like copper or gold to reduce eddy current losses.

In this paper on-chip three-dimensional inductor with high quality factor and inductance is proposed for RF and microwave subsystems. Section II contains experiment details, Section III contains application results, Section IV contains conclusion.

II. EXPERIMENT

In the design of on-chip inductor we have to consider conductor width, spacing between conductors, thickness of conductors, number of turns and distance between layers of conductors. In literature many proposed expressions for the extraction of inductance value for on-chip inductors. Greenhouse method is the basic concept for all the inductance expressions in literature. The procedure for the extraction of inductance of multi-turn square planar on-chip inductor of rectangular cross-section for a coil or a part of a inductor of any shape is given as

\[ L = L_0 + \sum M \]

Where \( L \) is the total inductance, \( L_0 \) is the sum of the self-inductances of all the straight segments, and \( \sum M \) is the sum of the mutual inductances, both positive and negative. Mutual inductance is positive when current flow in two parallel conductors is in the same direction and negative when current flow is in opposite directions. From the basic concept the expression of Q-factor is \( Q = \frac{L}{R} \) as frequency increases, the value of R increases due to skin and proximity effects. As the line resistance increases the value of Q-factor decreases. Thus design is made in such a way to decrease the line resistance by increasing width of conductor. The shape of the proposed inductor is as shown in fig.3. The concept of proposed inductor is two layers are considered half turn of the conductor is placed in one layer and other half in another layer.

These conductors in two different layers are connected through conical “vias” with properties same as the conducting...
material which are separated by 5mm spacing. The proposed inductor is simulated in IE3D and analysis is carried out in EM field solver with the help of series RL and shunt RC lumped Pi model. The materials used in this structure are silicon as substrate material and copper as conducting material with moderate thickness. The properties of these materials are

i) Silicon with dielectric constant 12, loss tangent 0.015, permeability 1, Real part of conductivity 0.00156
ii) Metallic conductor as copper with dielectric constant 6, Loss tangent 0.0001, Permeability of $1.25 \times 10^{-6}$, Real part of conductivity $5.85 \times 10^7$.

The dimensions of the proposed inductors are width of conductor 0.8 mm, spacing between adjacent conductors is 0.2 mm, and spacing between layers is 5 mm. The basic structure of on-chip inductor and three dimensional on-chip inductor areas shown in fig.1 and fig.2 respectively. 3-D view of on-chip three dimensional inductor is shown in fig.3. Simulation of the proposed on-chip three dimensional inductor is carried out in IE3D by using meshing process and the response is obtained in terms of scattering parameters which are converted to Y parameters for obtaining Q-value. From these parameters using internal solving mechanism of lumped pi model the values of quality factor and inductance are obtained. Proposed on chip three dimensional inductor is compared with on chip planar inductor.

A. Quality factor:

From the results as shown in figure 5 it can be observed that the on-chip three dimensional inductor has better quality factor than on chip planar inductor for the proposed frequency range of 30MHz to 100 MHz. Proposed on chip three dimensional inductor has 47-162% improvement in quality factor value when compared to basic on chip planar inductor.
B. Inductance:

From the results as shown in figure 5 it can be observed that on chip three dimensional inductor has better inductance value w.r.t on chip planar inductor for the proposed frequency range of 30MHz to 100 MHz. Proposed on chip three dimensional inductor has 18-28% improvement in inductance value when compared to basic on chip planar inductor.

The achievement of this higher order quality factor and inductance will make proposed inductor to perform in a better manner for an enhanced frequency behavior. Hence this inductor can be used in wide range of wireless applications by placing in circuits like filters, Phase Locked Loop and Voltage Controlled Oscillator.

III. FILTER APPLICATION

In communication system, the first block is filter circuit which allows tuned frequency and suppress remaining signals. For this operation we use band pass filter that allows certain range of band frequencies in the spectrum. In general band pass filter is a combination of low pass and high pass filters. The bandwidth of the filter mainly depends on quality factor of the inductor we are using.

Tank circuit we are using will resonate at one particular frequency where we call it as self resonant frequency. This also acts as centre frequency for the amplitude response. The bandwidth of the filter mainly depends on Q-factor. The relation is inverse, where Q-factor increases bandwidth decreases. Depending on requirement we choose Q-factor value which decides bandwidth of the system. It may be narrow band filter or wide band filter. For present RF applications we need narrow band filter. The response of band pass filter for the inductance values obtained in the simulation result is shown in fig 7. From fig 7 it can be observed that amplitude response of proposed inductor has better result when compared with on chip planar inductor.
IV. CONCLUSION

An on-chip three dimensional inductor using multi layer concept is proposed in this paper. The performance of the proposed three dimensional inductor is compared with planar inductor. From the experimental results the proposed on-chip three dimensional inductor has Q-factor of (47-162) % improvement and inductance value of (18-28) % improvement in the frequency range of (30-100) MHz w.r.t planar inductor in the area of cross-section 10×10 mm² of CMOS technology.

REFERENCES


